3.3V-Supply RS-485 with IEC ESD Protection

Check for Samples: SN65HVD72, SN65HVD75, SN65HVD78

FEATURES

- **Small-size MSOP or SON Packages Save Board Space, or SOIC for Drop-in Compatibility**
- **Bus I/O Protection**
  - **> ±15kV HBM protection**
  - **> ±12kV IEC61000-4-2 Contact Discharge**
  - **> ±12kV IEC61000-4-2 Air-Gap Discharge**
- **Extended Industrial Temperature Range –40°C to 125°C**
- **Large Receiver Hysteresis (80 mV) for Noise Rejection**
- **Low Unit-loading allows over 200 connected nodes**
- **Low Power Consumption**
  - **Low Standby Supply Current: < 2 µA**
  - **I_{CC} <1 mA Quiescent During Operation**
- **5V-Tolerant Logic Inputs Compatible With 3.3 V or 5 V Controllers**
- **Signaling Rate Options Optimized for: 250 kbps, 20 Mbps, 50 Mbps**

APPLICATIONS

- **Factory Automation**
- **Telecomm Infrastructure**
- **Motion Control**

DESCRIPTION

These devices have robust 3.3V drivers and receivers in a small package for demanding industrial applications. The bus pins are robust to ESD events, with high levels of protection to Human-Body Model and IEC Contact Discharge specifications.

These devices each combine a differential driver and a differential receiver, which operate from a single 3.3-V power supply. In the half-duplex devices, the driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. In the full-duplex devices, the driver differential outputs and the receiver differential inputs are separate pins, to form a bus port suitable for full-duplex (four-wire bus) communication. Full-duplex devices are available in compact 8-pin always-enabled versions, or with separate driver and receiver enables. These devices all feature a wide common-mode voltage range making the devices suitable for multi-point applications over long cable runs. These devices are characterized from -40°C to 125°C.

Table 1. Product Selection Guide

Part Number	Signaling Rate	Cable Length	Duplex	Enables	Package	Status
SN65HVD72	up to 250 kbps	up to 2000 m	Half	DE, RE	MSOP-8 SOIC-8	Preview
SN65HVD75	up to 20 Mbps	up to 100 m	Half	DE, RE	MSOP-8 SOIC-8	Preview Available
SN65HVD78	up to 50 Mbps	up to 50 m	Half	DE, RE	MSOP-8 SOIC-8	Preview

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SN65HVD72, 75, 78

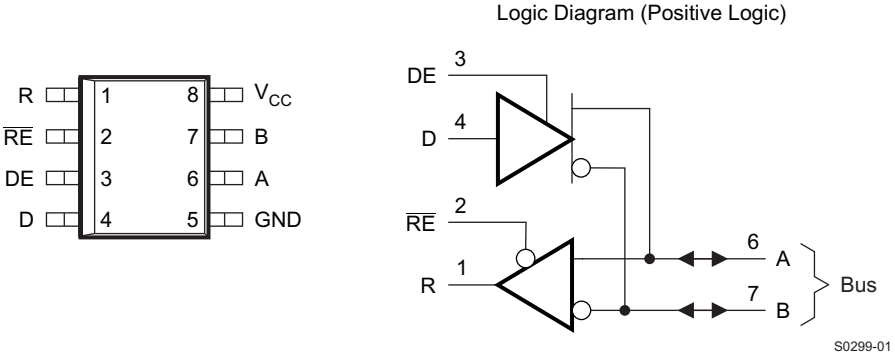


Table 2. DRIVER FUNCTION TABLE

INPUT	ENABLE	OUTPUTS		
D	**DE**	**A**	**B**	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus High by default

Table 3. RECEIVER FUNCTION TABLE

DIFFERENTIAL INPUT	ENABLE	OUTPUT	
$V_{ID} = V_A - V_B$	**RE**	**R**	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	fail-safe high output
Idle (terminated) bus	L	H	fail-safe high output

ABSOLUTE MAXIMUM RATINGS(1)

	VALUE		UNIT
	MIN	MAX	
Supply Voltage, V_{CC}	–0.5	5.5	V
Voltage range at A or B Inputs	–8	18	V
Input voltage range at any logic pin	–0.3	5.7	V
Voltage input range, transient pulse, A and B, through 100Ω	–100	100	V
Receiver Output Current	–24	24	mA
Junction Temperature, T_J		170	°C
Continuous total power dissipation	See the Thermal Characteristics table		
IEC 61000-4-2 ESD (Air-Gap Discharge), bus terminals and GND		±12	kV
IEC 61000-4-2 ESD (Contact Discharge), bus terminals and GND		±12	kV
IEC 60749-26 ESD (Human Body Model), bus terminals and GND		±15	kV
JEDEC Standard 22, Test Method A114 (Human Body Model), all pins		±8	kV
JEDEC Standard 22, Test Method C101 (Charged Device Model), all pins		±1.5	kV
JEDEC Standard 22, Test Method A115 (Machine Model), all pins		±300	V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_I	Input voltage at any bus terminal (separately or common mode) (1)		–7		12	V
V_{IH}	High-level input voltage (Driver, driver enable, and receiver enable inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (Driver, driver enable, and receiver enable inputs)		0		0.8	V
V_{ID}	Differential input voltage		–12		12	V
I_O	Output current, Driver		–60		60	mA
I_O	Output current, Receiver		–8		8	mA
R_L	Differential load resistance		54	60		Ω
C_L	Differential load capacitance			50		pF
$1/t_{UI}$	Signaling rate	HVD72			250	kbps
		HVD75			20	Mbps
		HVD78			50	Mbps
T_A	Operating free-air temperature (See the application section for thermal information)		–40		125	°C
T_J	Junction Temperature		–40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60 Ω, 375 Ω on each output to -7 V to 12 V		See	1.5			V
		R_L = 54 Ω (RS-485)		See	1.5	2		V
		R_L = 100 Ω (RS-422) $T_J \geq 0°C$, $V_{CC} \geq 3.2V$			2	2.5		V
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage	R_L = 54 Ω, C_L = 50 pF			–50	0	50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	Center of two 27-Ω load resistors		See	1	$V_{CC}/2$	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage				–50	0	50	V
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage					500		mV
C_{OD}	Differential output capacitance					30		pF
V_{IT+}	Positive-going receiver differential input voltage threshold				See (1)	–70	–20	mV
V_{IT-}	Negative-going receiver differential input voltage threshold				–200	–150	See (1)	mV
V_{HYS}	Receiver differential input voltage threshold hysteresis ($V_{IT+} – V_{IT-}$)				50	80		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –8 mA			2.4	V_{CC}–0.3		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA				0.2	0.4	V
I_I	Driver input, driver enable, and receiver enable input current				–2		2	µA
I_{OZ}	Receiver output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ at V_{CC}			–10		10	µA
I_{OS}	Driver short-circuit output current				–160		160	mA
I_I	Bus input current (disabled driver)	V_{CC} = 3 to 3.6 V or V_{CC} = 0 V, DE at 0 V	HVD72, 75	V_I = 12 V		75	150	µA
				V_I = –7 V	–100	–40		µA
			HVD78	V_I = 12 V		150	333	µA
				V_I = –7 V	–267	–120		µA
I_{CC}	Supply current (quiescent)	Driver and Receiver enabled	DE=V_{CC}, RE=GND, No load				950	µA
		Driver enabled, receiver disabled	DE=V_{CC}, RE=V_{CC}, No load				500	µA
		Driver disabled, receiver enabled	DE=GND, RE=GND, No load				800	µA
		Driver and receiver disabled	DE=GND, D=open RE=V_{CC}, No load			0.01	2	µA
	Supply current (dynamic)	See the TYPICAL CHARACTERISTICS section						

(1) Under any specific conditions, V_{IT+} is assured to be at least V_{HYS} higher than V_{IT-}.

SWITCHING CHARACTERISTICS

250 kbps devices (HVD70, 71, 72) bit time > 4 µs (over recommended operating conditions)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	See	0.4		1	µs
t_{PHL}, t_{PLH}	Driver propagation delay				0.4	0.8	µs
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$				10	30	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See and		0.1	0.5	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			0.2	1	µs
		Receiver disabled			3	9	µs
RECEIVER							
t_r, t_f	Receiver output rise/fall time	C_L = 15 pF	See			30	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				100	195	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$				6	15	ns
t_{PLZ}, t_{PHZ}	Receiver disable time				15	500	ns
$t_{PZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled	See		80	130	ns
		Driver disabled	See		3	8	µs

SWITCHING CHARACTERISTICS

15 kbps devices (HVD73, 74, 75) bit time > 65 ns (over recommended operating conditions)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	See	2		14	ns
t_{PHL}, t_{PLH}	Driver propagation delay			7		17	ns
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$					2	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See and			50	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled				20	ns
		Receiver disabled				7	µs
RECEIVER							
t_r, t_f	Receiver output rise/fall time	CL = 15 pF	See			10	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time					70	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$					6	ns
t_{PLZ}, t_{PHZ}	Receiver disable time				15	30	ns
$t_{pZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled	See			50	ns
		Driver disabled	See		3	8	µs

SWITCHING CHARACTERISTICS

50 kbps devices (HVD76, 77, 78) bit time > 20 ns (over recommended operating conditions)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	See	1		6	ns
t_{PHL}, t_{PLH}	Driver propagation delay					9	ns
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$					0.6	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See and			130	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled				40	ns
		Receiver disabled				85	µs
RECEIVER							
t_r, t_f	Receiver output rise/fall time	CL = 15 pF	See	1		3.5	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time					30	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$					2.5	ns
t_{PLZ}, t_{PHZ}	Receiver disable time				15	200	ns
$t_{pZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled	See		25	60	ns
		Driver disabled	See		3	8	µs

PARAMETER MEASUREMENT INFORMATION

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50 Ω.

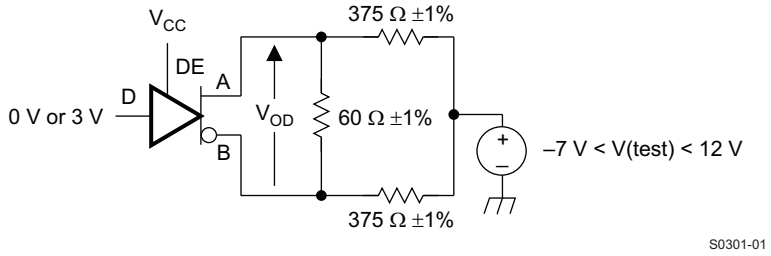


Figure 1. Measurement of Driver Differential Output Voltage with Common-Mode Load

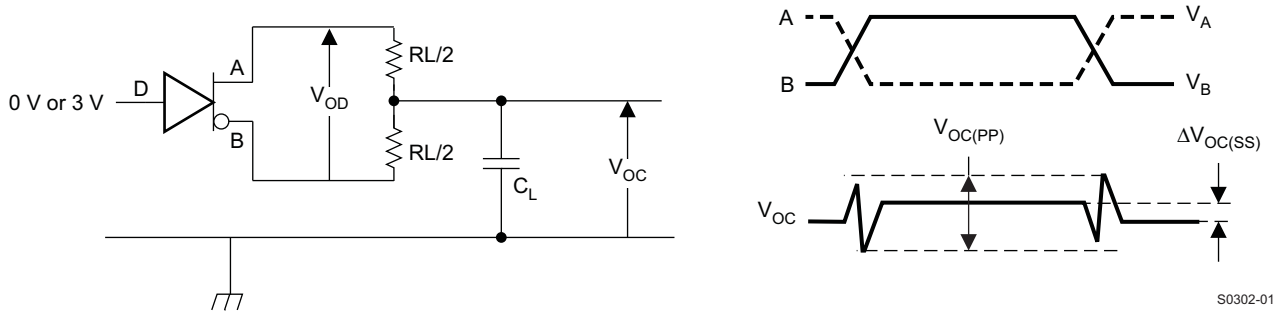


Figure 2. Measurement of Driver Differential and Common-Mode output with RS-485 Load

PARAMETER MEASUREMENT INFORMATION (continued)

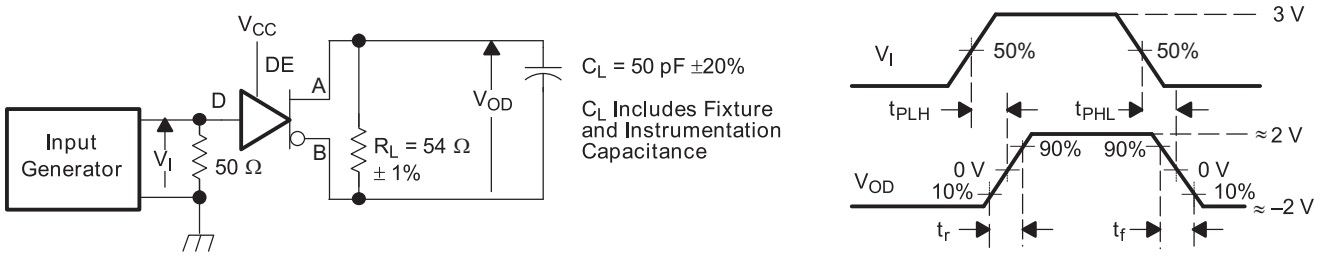
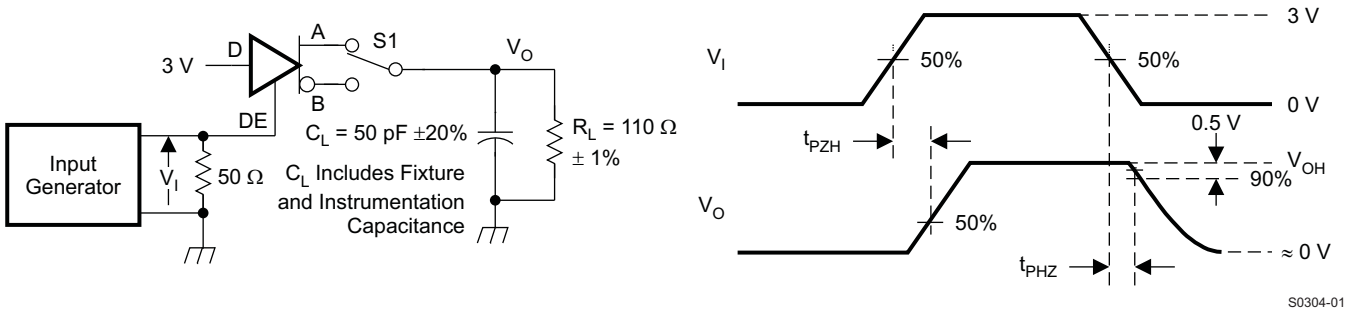
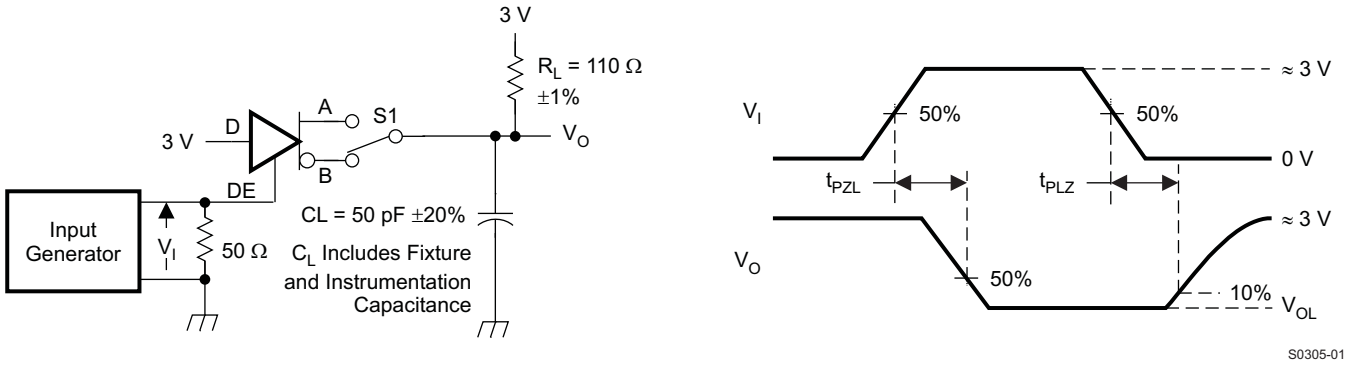


Figure 3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



D at 3 V to test non-inverting output, D at 0 V to test inverting output.

Figure 4. Measurement of Driver Enable and Disable Times with Active High Output and Pull-Down Load



D at 0V to test non-inverting output, D at 3V to test inverting output.

Figure 5. Measurement of Driver Enable and Disable Times with Active Low Output and Pull-Up Load

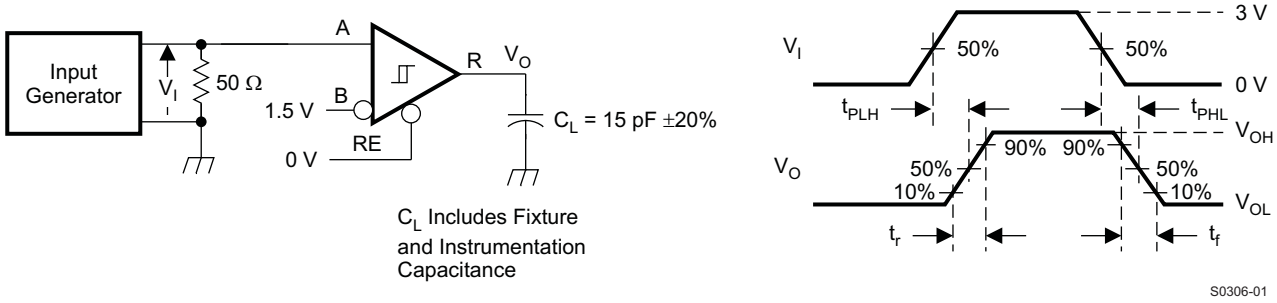


Figure 6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

PARAMETER MEASUREMENT INFORMATION (continued)

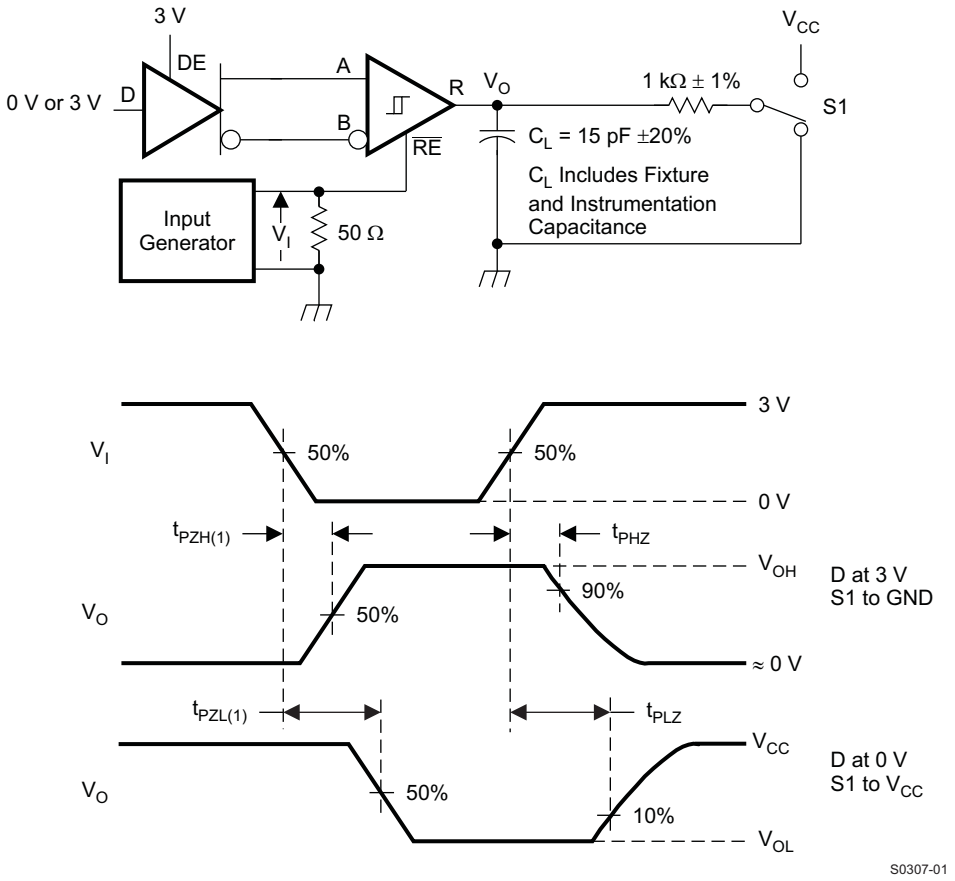


Figure 7. Measurement of Receiver Enable/Disable Times with Driver Enabled

PARAMETER MEASUREMENT INFORMATION (continued)

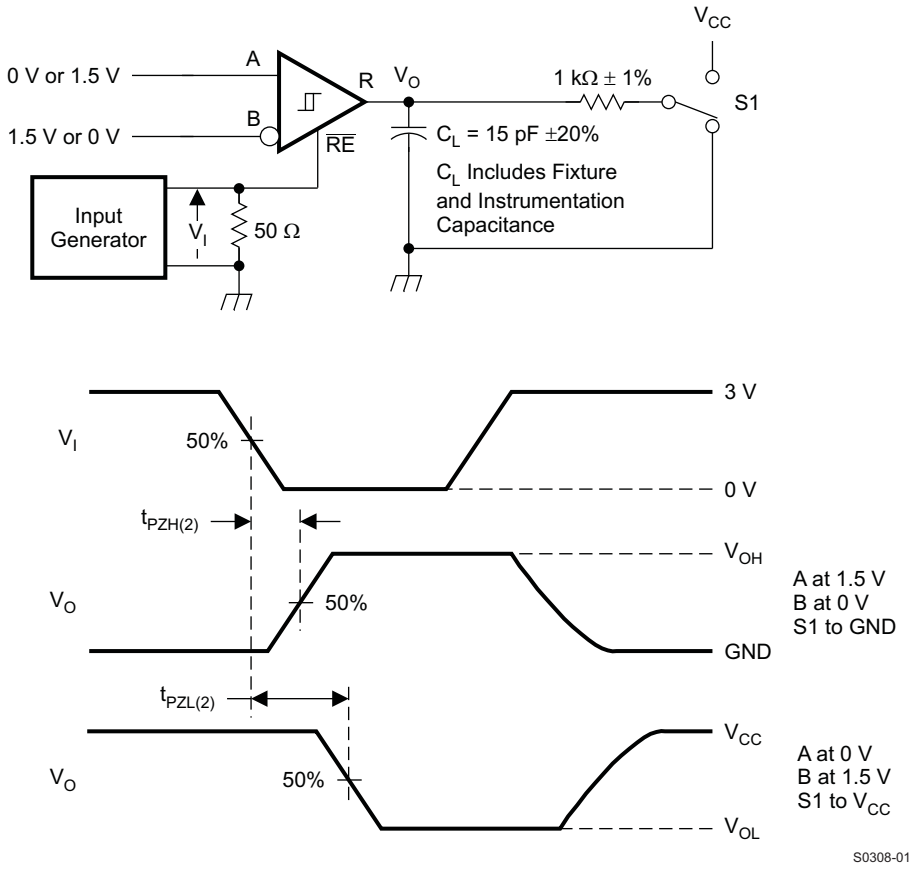


Figure 8. Measurement of Receiver Enable Times with Driver Disabled

TYPICAL CHARACTERISTICS

DRIVER OUTPUT VOLTAGE vs DRIVER OUTPUT CURRENT

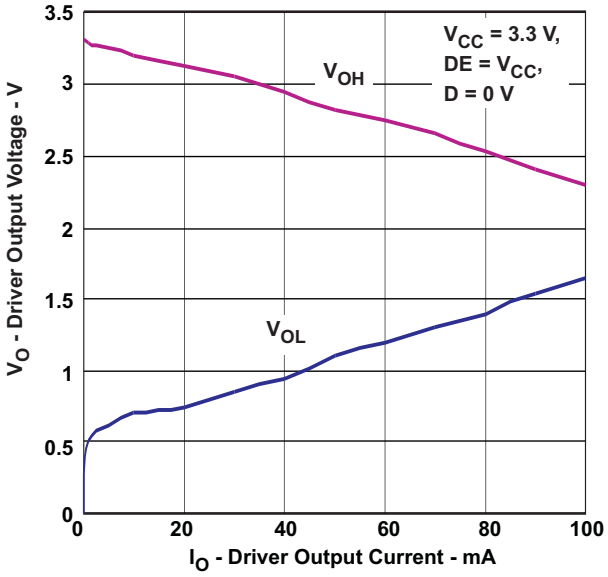


Figure 9.

DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs DRIVER OUTPUT CURRENT

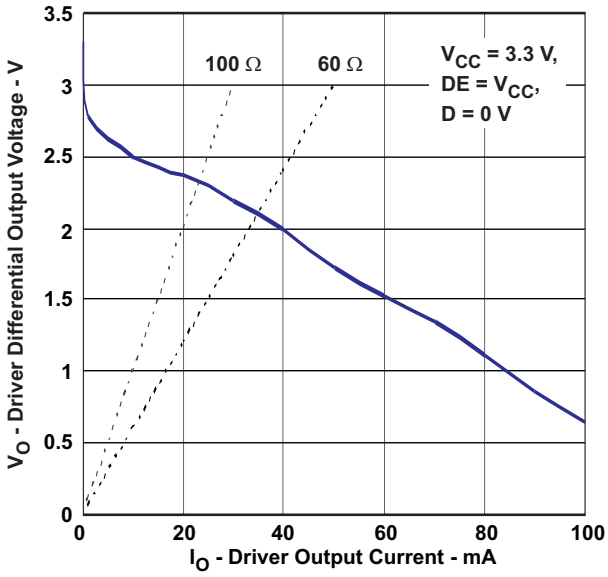


Figure 10.

DRIVER OUTPUT CURRENT vs SUPPLY VOLTAGE

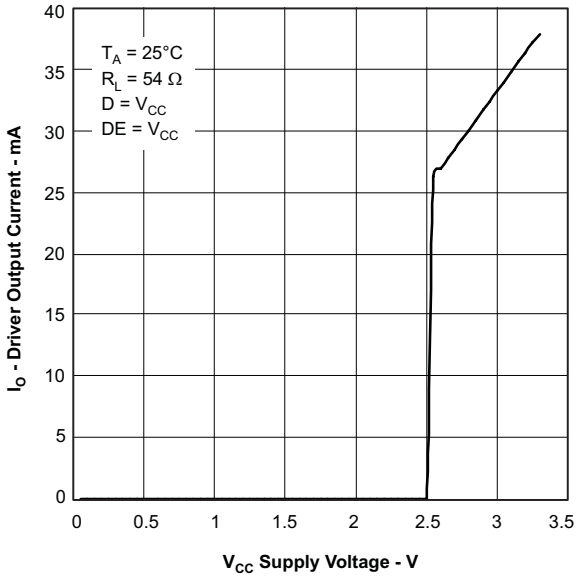


Figure 11.

DEVICE INFORMATION

Table 4. Thermal Characteristics

PARAMETER			TEST CONDITIONS	VALUE	UNITS
ΘJA	Junction-to-Ambient Thermal Resistance		JEDEC High-K model, SOIC-8	110.7	°C/ W
			JEDIC Low-K model		
ΘJB	Junction-to-Board Thermal Resistance		SOIC-8	51.3	°C/ W
ΘJC	Junction-to-Case Thermal Resistance		SOIC-8	54.7	°C/ W
PD	Power Dissipation: driver and receiver enabled, 50% duty cycle square-wave signal at signaling rate: HVD72 at 250 kbps HVD75 at15 Mbps HVD78 at 50 Mbps	3.3V supply Unterminated	V_{CC} = 3.6V, TJ = 150ºC, R_L = 300 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver)		mW
		3.3V supply RS-422 load	V_{CC} = 3.6V, TJ = 150ºC, R_L = 100 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver)		
		3.3V supply RS-485 load	V_{CC} = 3.6V, TJ = 150ºC, R_L = 54 Ω, C_L = 50 pF (driver), C_L = 15 pF (receiver)		
TSD	Thermal Shut-down Junction Temperature			170	°C

Receiver Failsafe

The differential receiver is “failsafe” to invalid bus states caused by:

- open bus conditions such as a disconnected connector
- shorted bus conditions such as cable damage shorting the twisted-pair together, or
- idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic High state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds so that the “input indeterminate” range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input V_{ID} is more positive than +200 mV, and must output a Low when the V_{ID} is more negative than -200 mV. The receiver parameters which determine the failsafe performance are V_{IT+} and $V_{IT-}$and V_{HYS}. As seen in the Electrical Characteristics table, differential signals more negative than -200 mV will always cause a Low receiver output. Similarly, differential signals more positive than +200 mV will always cause a High receiver output.

When the differential input signal is close to zero, it will still be above the V_{IT+} threshold, and the receiver output will be High. Only when the differential input is more negative than V_{IT-}will the receiver output transition to a Low state. So the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value V_{HYS} (the separation between V_{IT+} and V_{IT-}) as well as the value of V_{IT+}.

Signals which transition from positive to negative (or from negative to positive) will transition only once, ensuring no spurious bits.

PACKAGING INFORMATION

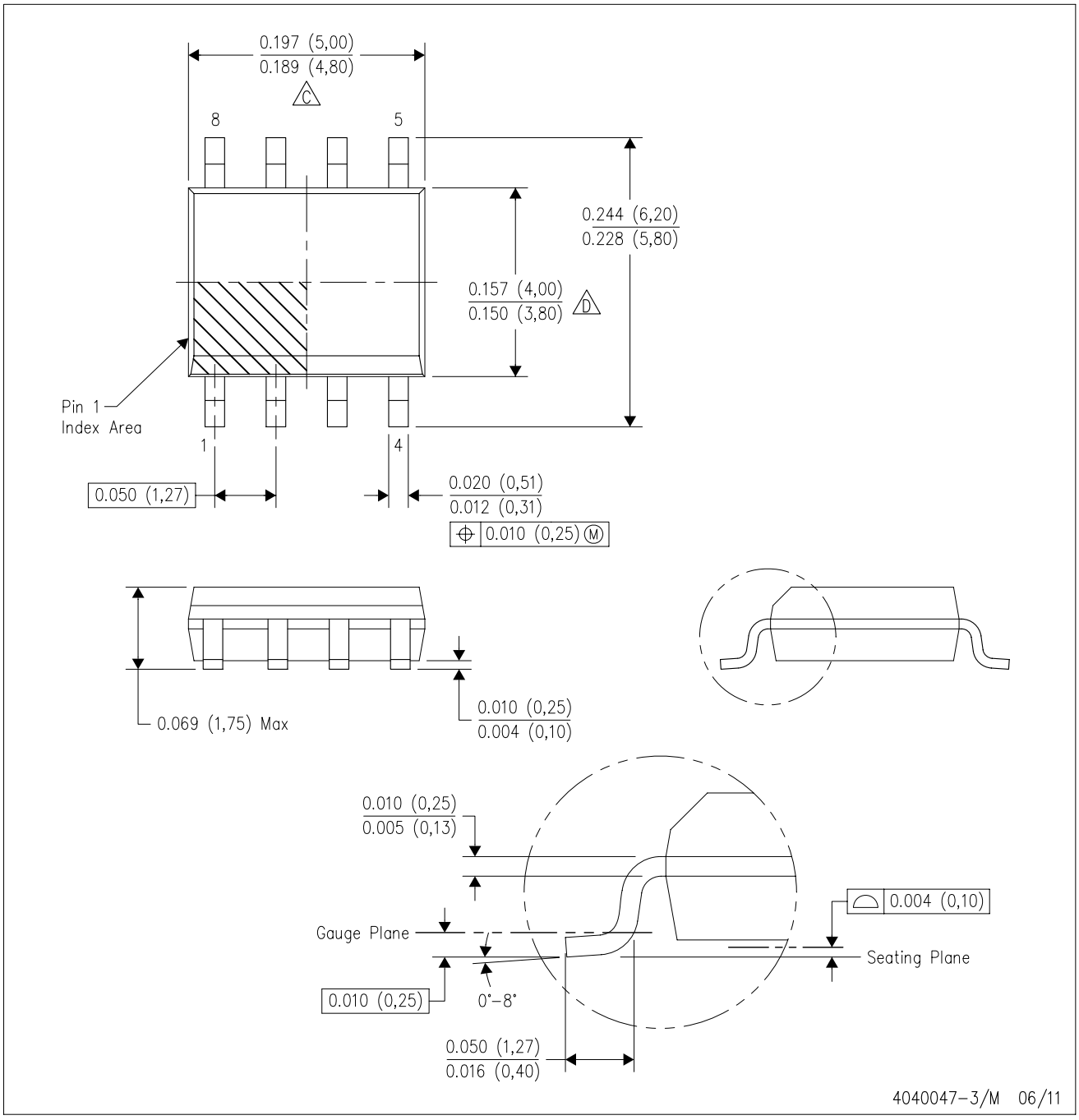
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN65HVD75D	PREVIEW	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN65HVD75DR	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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